No. AN9411 June 1994

Application Note

Using the HI1171 Evaluation Kit

Author: Stephen G. LaJeunesse

Introduction

The HI1171 is an 8-bit 40MHz Digital to Analog Converter. This device is TTL/CMOS logic compatible. This current out DAC is ideally suited for Video Signal Reconstruction and low cost DDS (Direct Digital Synthesis) applications due to the inherent low noise design and low glitch area.

Description

Architecture

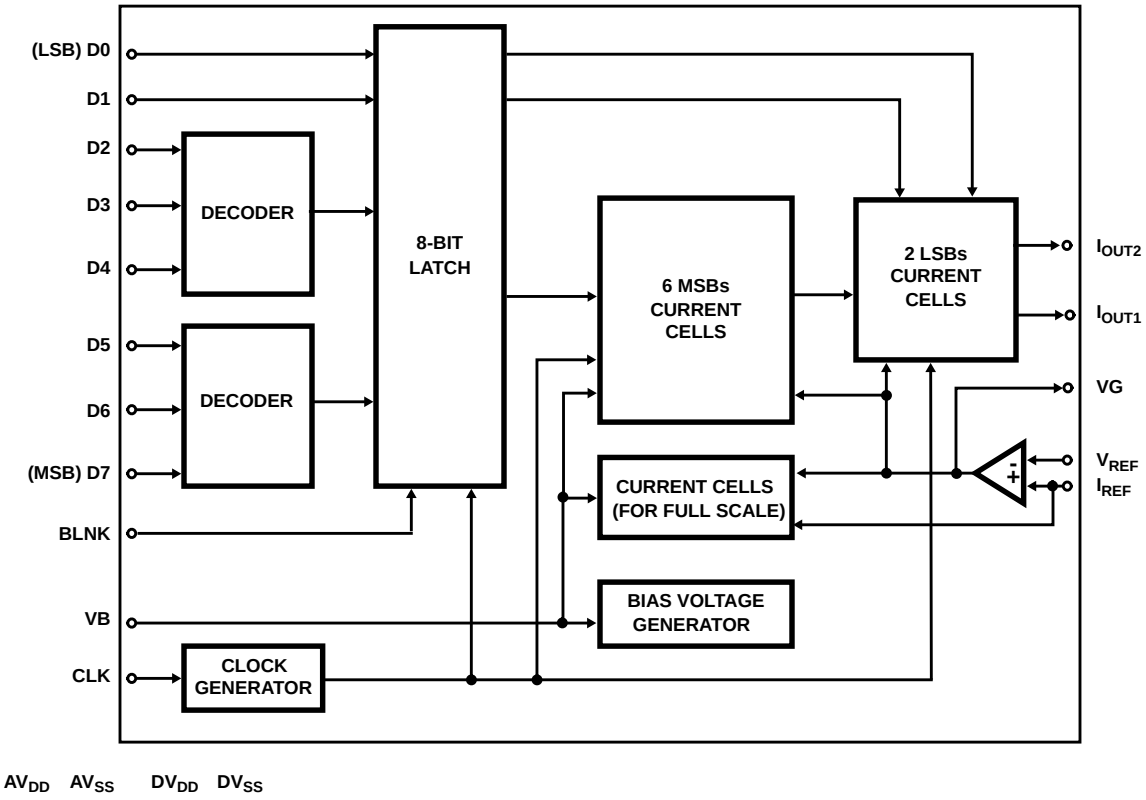
The HI1171 DAC is a binaurally weighted current cell architecture. The Functional Block Diagram shows the functional architecture of the device. The internal latches have a blanking function that clears the data in the 8-bit latch and holds the output current at zero. An external reference must be used. The HI1171 is internally referenced to the +5V supply to reduce internal noise. As such, an external potentiometer can be used to derive a reference voltage.

The I_{REF} pin is used to set the scalable output current. In setting the output current the IREF pin should have a resistor connected to it that is 16 times greater than the output resistor.

$$R_{REF} = 16 \times R_{OUT}$$

As the values of both R_{OUT} and R_{REF} increase, power consumption is decreased, but glitch energy and output settling time is increased.

Functional Block Diagram



Measuring Glitch

Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time. Unequal delay paths through the device can also cause one current source to change before another. To minimize this, the Intersil HI1171 employs an internal register, just prior to the current sources, that is updated on the clock edge. In traditional DACs, the worst case glitch usually happens at the major transition i.e. 0111 1111 to 1000 0000.

Since the glitch is a transient event, this leads designers to believe that a simple low pass filter can be used to eliminate or reduce the size of the glitch. In effect, low pass filtering a glitch tends to “smear” the event and does little to remove the energy of the transient. See Figure 1.

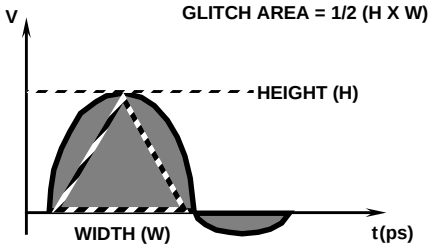


FIGURE 1. GLITCH AREA

Integral Linearity

The HI1171 has a FSR range of 15mA. When driving an equivalent 75Ω load the full scale voltage swing is 0 to +1.125V. Most video and communication applications use a $1V_{P-P}$ voltage swing which yields 13mA full scale current sink capability. With a $1V_{P-P}$ voltage swing on the HI1171 output, an LSB is

$$\text{LSB} = \text{Full Scale Range}/2^{N} - 1$$

where N is the number of bits and the Full Scale Range is 1V.

The LSB size for this application is 3.9mV. To determine the Integral Linearity of the HI1171 the bit weights of each major transition is taken. Since the End Point method is used to calculate the overall INL the first measurements taken are Offset and then the Full Scale Voltage. Then the ideal LSB size for this given End Point line is used to calculate the INL error.

The worst case linearity of the HI1171 is specified to be less than +1.3 and -0.5 LSBs. For the overall transfer function the typical INL performance is shown in Figure 2.

Differential Linearity and Missing Codes

For a D/A Converter the differential linearity is the step size difference through-out the entire code range. For the HI1171 the step to step maximum difference is ±0.25 LSBs. For any given D/A converter, to guarantee no missing codes the converter must be monotonic.

The definition of Monotonicity is that as the input code is increased the output should increase. When an input code is increased and the output of the DAC does not increase or reverses direction then this converter is assumed to be missing codes. As shown in Figure 3 as the input code increases the output voltage should increase. When an error of 1.0 LSB is incurred that bit can be assumed to be a missing code since the output did not increase but rather remained the same.

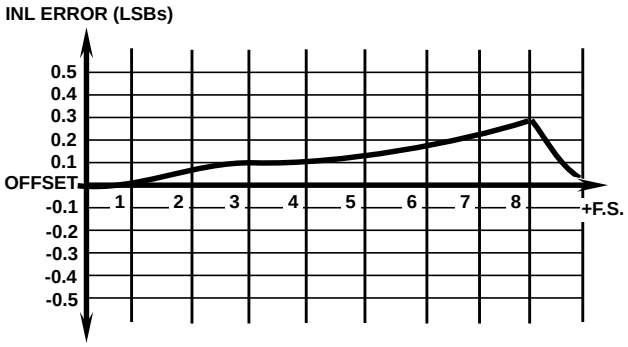


FIGURE 2. INL TYPICAL PERFORMANCE CURVE

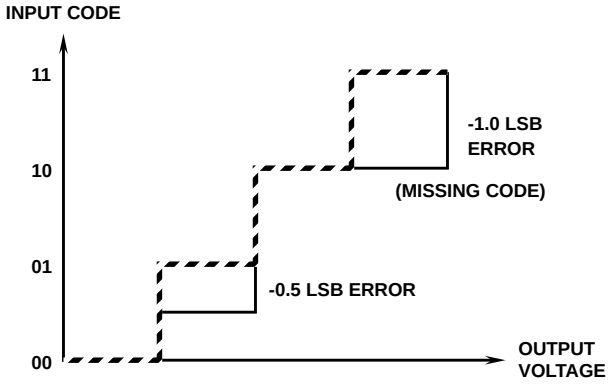


FIGURE 3. DNL EXAMPLE

The Evaluation Board

The HI1171 Evaluation board is a 1/2 size daughter board designed to interface to the HSP-EVAL board. These boards when used together create a flexible and powerful DDS system. The HSP45116 board is used to generate the high speed digital SINE wave patterns for the D/A module. The HI1171 board reconstructs the incoming digital data to an analog representation that can be analyzed on a spectrum analyzer or oscilloscope.

Plugging In

After opening the HSP45116 board and the HI1171 board power should be applied to the banana jacks. A +5V supply will be needed. To reduce noise the power supply leads should be twisted pairs.

The interface cable should be connected to an IBM PC or compatible parallel port. Power should be applied to the board and then the software can be started. the software can be run directly from floppy disk. To run the software place the floppy disk into drive A: and type:

A: NCOMCTRL

the HSP45116 Control Panel will be loaded. To exercise the board the following parameters should be set:

BINFMT# = 0

and then set the Center Frequency to:

CENTER FREQUENCY = 01000000_H

where the center frequency is in hex. At this point the output of the HI1171 DAC module should be converting a SINE wave at 48kHz. Connect the output of the HI1171 module to an oscilloscope. Adjust the potentiometer until the output waveform has an amplitude of $1V_{P-P}$. Adjusting the potentiometer Clockwise (CW) will reduce the amplitude and Counter-Clockwise (CCW) will increase the amplitude.

The HI1171 module has a jumper plug for selecting the blanking feature of the HI1171. When J2 is installed, the DAC will not blank but will convert the incoming data. When J2 is not installed, the DAC will be blanked.

The HI1171 is very sensitive to clock noise. Some TTL/CMOS oscillators have tremendous amounts of ringing and overshoot. To reduce this use a clean clock source whenever possible.

Spurious Free Dynamic Range

The Spurious Free Dynamic Range of the HI1171 DAC is the most important specification for communication applications. This specification shows how Integral Linearity, Glitch, and Switching noise affect the spectral purity of the output signal. Several important things must be noted first.

When a quantized signal is reconstructed, certain artifacts are created. Let's take the example of trying to recreate a 1MHz Sine wave with a $1V_{P-P}$ output. In the frequency domain the fundamental should appear at 1MHz as shown in Figure 4.

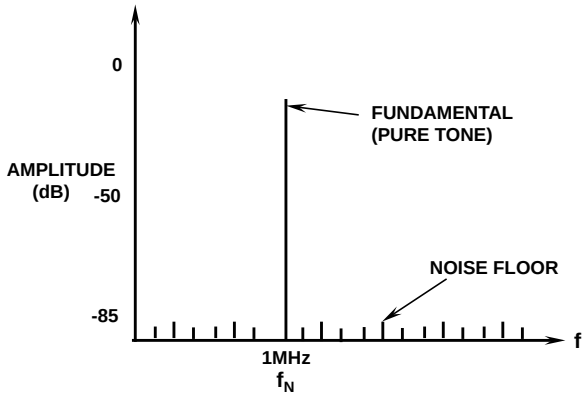


FIGURE 4. FREQUENCY PLOT OF 1MHz TONE

The fundamental of a pure 1MHz tone should appear as an impulse in the frequency domain at 1MHz. In a sampled system noise terms are produced near the sampling frequencies called aliases. These aliases are related to the fundamental in that they are located f_N around the sampling frequency as shown in Figure 5.

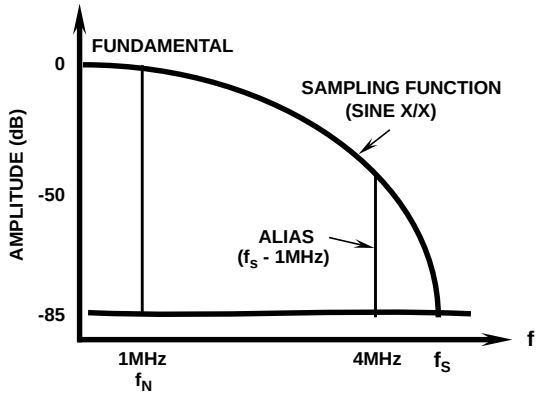


FIGURE 5. SAMPLING ALIAS PRODUCTS

So for a 1MHz fundamental and a 5MHz sampling rate an alias term is created at 4MHz. A SYNC2 function shaping is also induced by sampling a signal. Aliases continue up through the frequency spectrum repeating around the sampling frequency and its harmonics (i.e. $2f_S$, $3f_S$, $4f_S$...).

A reconstructed Sine wave out of the HI1171 is not ideal and as such has harmonics of the fundamental. The difference between the magnitude of the fundamental and the highest noise spur whether it is harmonically related to the fundamental or not, is the definition of Spurious Free Dynamic Range. Figures 6, 7, and 8 are sample Spectrum Analyzer plots taken, of the HI1171 at various frequencies. Included are the oscilloscope plots.

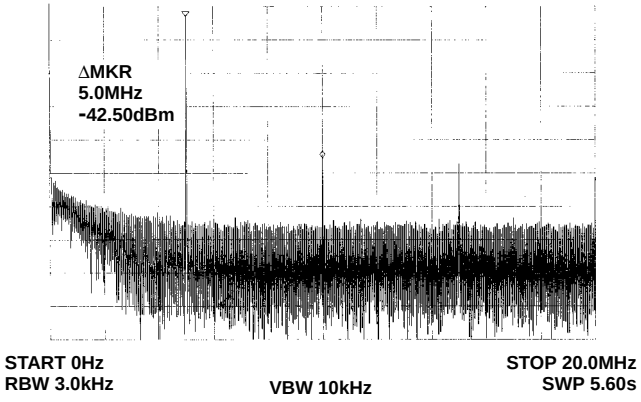


FIGURE 6A. SFDR TO NYQUIST UNFILTERED

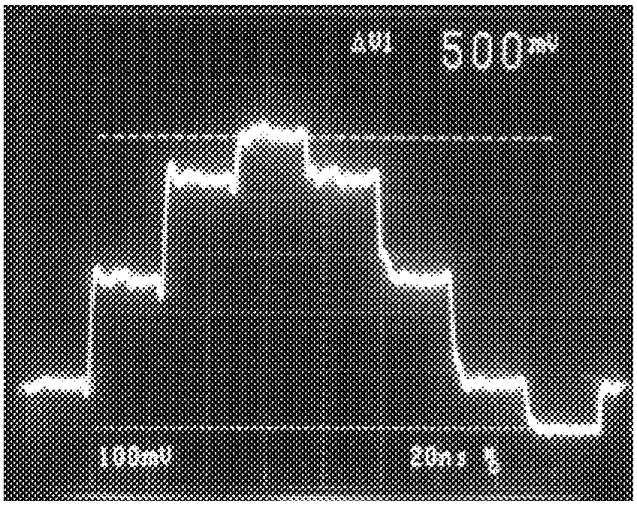


FIGURE 6B. 5MHz UNFILTERED OSCILLOSCOPE PLOT

FIGURE 6.

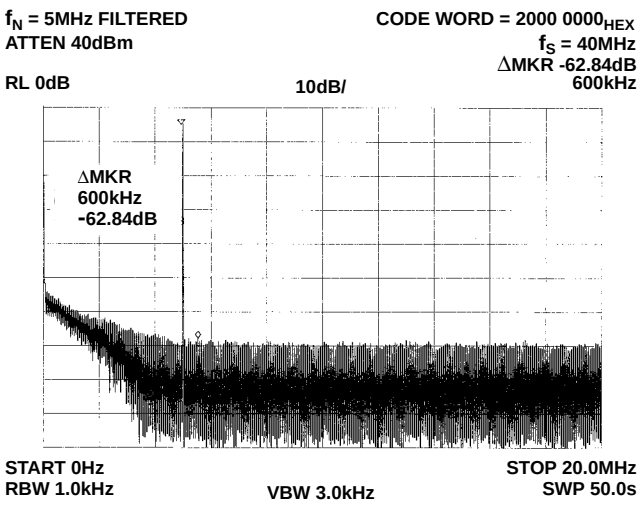


FIGURE 7A. SFDR TO NYQUIST BANDPASS FILTERED

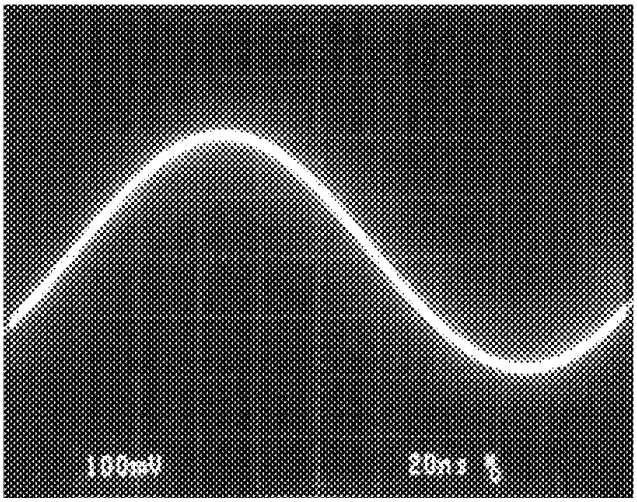


FIGURE 7B. 5MHz FILTERED OSCILLOSCOPE PLOT

FIGURE 7.

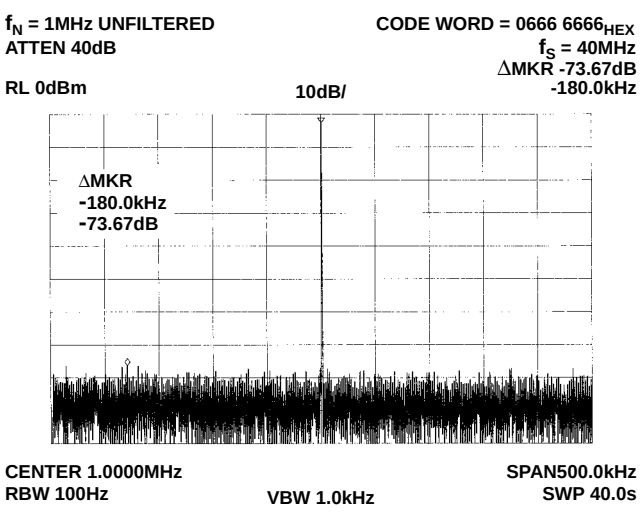


FIGURE 8A. LIMITED SPAN

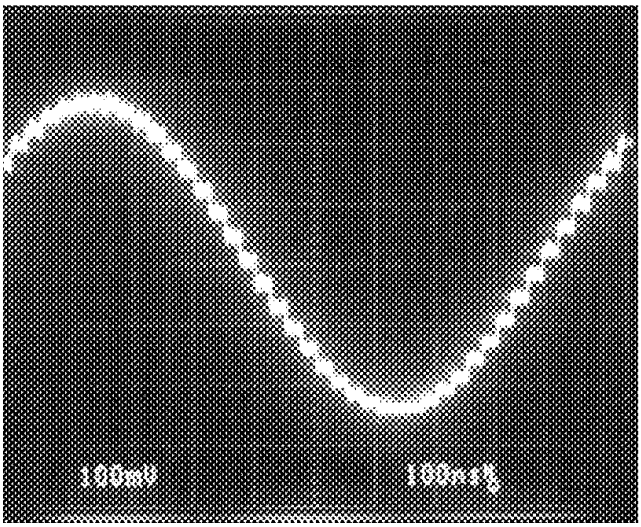


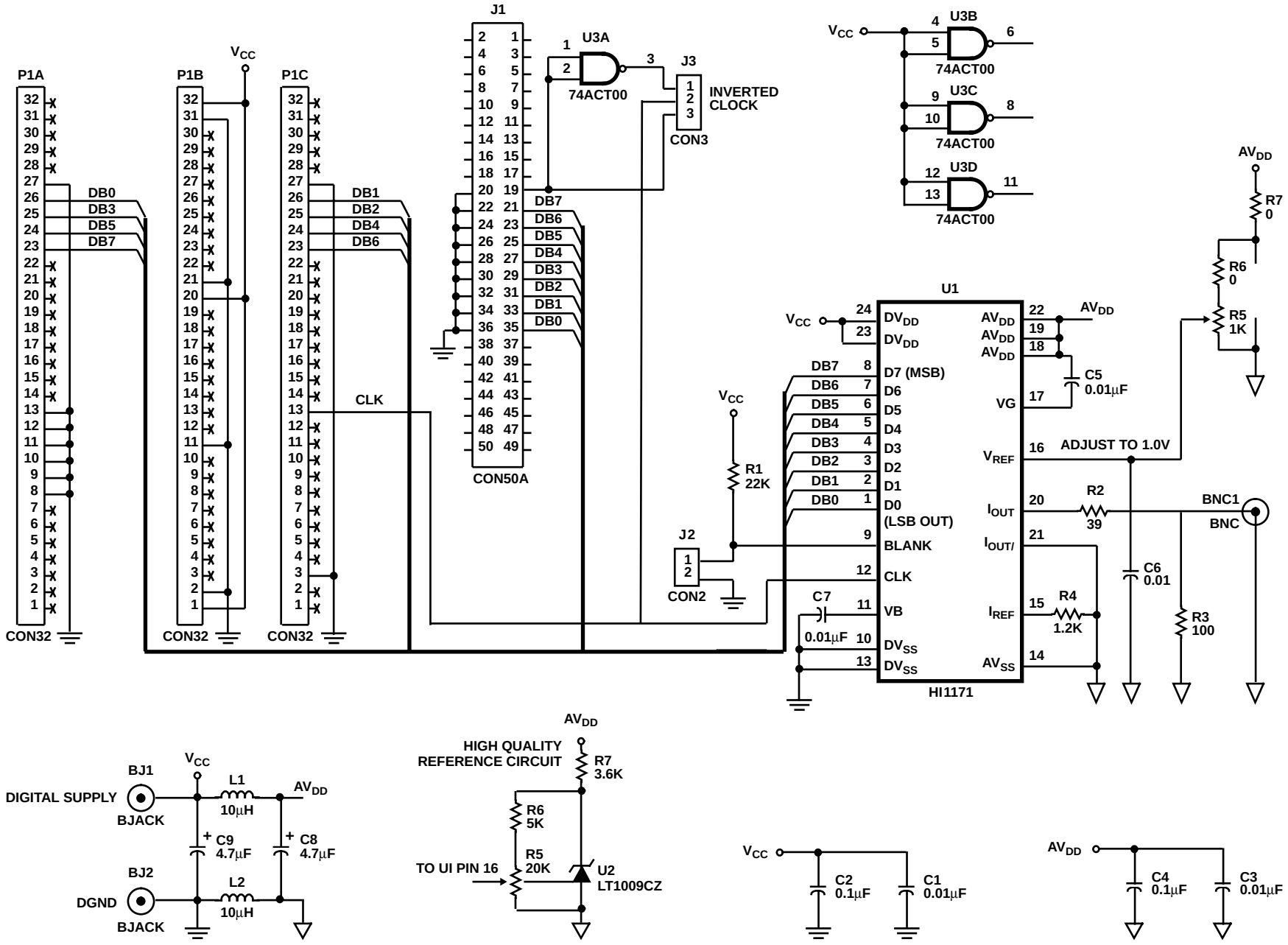
FIGURE 8B. 1MHz UNFILTERED OSCILLOSCOPE PLOT

FIGURE 8.

Schematic Materials List

PIN NUMBER	DESCRIPTION	PART NUMBER	VENDOR	QUANTITY	REFERENCE (DES)
1	96 Pin Female DIN	A1262-ND	Digi-Key	1	P1
2	2 Post Jumper Thru-Hole	518-1070	Allied	1	J2
3	Banana Jacks	J147-ND	Digi-Key	2	BJ1, 2
5	Female BNC Connector	713-7160	Allied	1	BNC1
6	50Ω Res. Thru-Hole	297-4157	Allied	1	R8
7	1.2kΩ Res. Thru-Hole	297-5366	Allied	1	R4
8	39Ω Res. Thru-Hole	297-5140	Allied	1	R2
9	100Ω Res. Thru-Hole	297-4202	Allied	1	R3
10	0Ω Res. Thru-Hole	-	-	2	R6, 7
11	22kΩ Res. Thru-Hole	297-4586	Allied	1	R1
12	1kΩ Pot	-	-	1	R5
12	10µH Ind. Thru-Hole	274300111	Dexter	2	L1, 2
13	0.1µF Cap CER Thru-Hole	852-1170	Allied	2	C2, 4
14	0.1µF Cap CER Thru-Hole	852-1157	Allied	5	C1, 3, 5, 6, 7
15	10µF TANT Cap Thru-Hole	926-1985	Allied	2	C8, 9
16	HI1171 D/A DIP Package	HI1171JIP	Intersil	1	U1
17	HI1171 Eval Board	HI1171.EVAL	-	1	-

Schematic Diagram



Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029